REMARKS

Applicants note the filing of a Supplemental Information Disclosure Statement herein on January 11, 2002 and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicants respectfully request that the information cited on the PTO-1449 be made of record herein and that an initialed copy of the PTO-1449 evidencing the same be returned to the undersigned attorney.

The Final Office Action mailed March 7, 2002, has been received and reviewed. Claims 1 through 23 and 36 through 49 are currently pending in the application. Claims 1 through 23, and 36 through 49 stand rejected. Applicants propose to amend claims 1, 18, 19 and 36 through 41, and respectfully request reconsideration of the application as proposed to be amended herein.

35 U.S.C. § 112 Claim Rejections

Claims 1 through 17, 36 through 40, and 41 through 49 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Applicants have amended the claims to remove the "unitary structure" language that was unclear to the Examiner. In light thereof, Applicants respectfully request the rejection of claims 1 through 17, 36 through 40 and 41 through 49 under 35 U.S.C. § 112, second paragraph be withdrawn.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Japanese Patent No. 10189653 to Kuniaki

Claims 1 through 5, 8, 10, 13 through 16, 36, and 40 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kuniaki (Japanese Patent No. 10189653). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers* v.

Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Kuniaki discloses a semiconductor element 3 that can be easily subjected to flip-chip mounting to a circuit board and is suitable for high-density mounting. A plurality of electrodes 7, which are to be directly bonded to the circuit board by way of solder balls 11 placed on top thereof, are arranged centrally in-line on semiconductor element 3 (see Figs. 1-7). Auxiliary electrodes 10a-d having the same form and size as electrodes 7 are arranged at various locations on the element surface 4a. Support projections 12 on auxiliary electrodes 10a-d, which are solder balls having the same form and size as solder balls 11, come into contact with the circuit board upon positioning the semiconductor element 3, and prevent movement of the semiconductor element 3 along an axis extending through each of the solder balls on the center part of the element surface 4a (see Abstract, lines 12-19).

Independent claim 1, as amended herein, recites the limitation of "forming at least one stabilizer comprising a dielectric material and securing said at least one stabilizer to said active surface". Amended independent claim 36 recites the limitation of "forming at least one stabilizer structure comprising a dielectric material". Kuniaki does not expressly or inherently describe a stabilizer formed of a dielectric material, but rather support projections 12 that are formed as conductive solder balls. Therefore, Applicants respectfully submit Kuniaki does not expressly or inherently describe each and every element of claims 1 and 36, and under 35 U.S.C. § 102(b) they are allowable over the cited reference.

Claims 2 through 5, 8, 10, 13 through 16 and 40 are allowable, among other reasons, as depending from independent claim 1, which is allowable.

Claim 8 is further allowable because Kuniaki neither expressly nor inherently describes forming a stabilizer to be securable to a sealing material on an active surface of at least one flip-chip semiconductor die. Instead, the support projections of Kuniaki are formed on auxiliary electrodes 10a-d.

Claim 14 is additionally allowable since Kuniaki lacks any express or inherent description of positioning at least one stabilizer so as to avoid contact with conductive traces on a carrier substrate.

Claim 40 is allowable, among other reasons, as depending from claim 36, which is allowable.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki in view of U.S. Patent No. 4,575,330 to Hull

Claims 6, 7, 11, and 37 through 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653) in view of Hull (U.S. Patent No. 4,575,330). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

Claims 6, 7, and 10 are each allowable, among other reasons, as depending from claim 1, which is allowable.

Claims 37 through 39 are each allowable, among other reasons, as depending from claim 36, which is allowable.

Further, Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections of claims 6, 7, 11, and 37 through 39 are improper because they fail to establish a *prima facie* case of obviousness.

As described above, Kuniaki describes a semiconductor element 3 having auxiliary electrodes 10a-d with solder ball support projections 12 thereon to support the semiconductor element 3 in flip-chip attachment.

Hull teaches an apparatus for production of three dimensional objects by stereolithography. The discussion of Hull is directed to simplified means for rapid *prototyping* of parts to allow quickly and economically moving from a design stage to production (see col. 1, line 63, to col. 2, line 12). There is no suggestion or motivation in the cited references or from the knowledge generally available in the prior art which would lead one of ordinary skill in the art to modify Kuniaki with the teachings of Hull as has been presented.

The Examiner states that Hull discloses forming a three-dimensional object for a microelectronic device, and that one of ordinary skill would be motivated to combine the two inventions because one could precisely form the stabilizers in a densely packed package without risk of short circuiting. First, Applicants can find no evidence in Hull describing forming parts for microelectronic devices. In fact, the only mention of microelectronics is made as an example of uses for reproducing *graphic* objects using techniques such as photographic reproduction, xerography, and microlithography (see col. 4, lines 43-50). Second, Hull does not provide any description of forming parts which are secured or attached to other items not formed by stereolithography, such as would be the case with the instant combination. Hull envisions providing prototypes by creating an entire assembly using stereolithography. Finally, it is unclear how stereolithographically formed supports would significantly reduce the risk of short circuiting during construction of the Kuniaki flip chip assembly. The same steps for forming the support projections 12 and electrodes 10a-d would still be required to make the conductive electrodes 7 and solder balls 11, and the short circuiting risks during construction would therefore not be eliminated.

Accordingly, there is no suggestion in Hull, Kuniaki or from any knowledge generally available in the prior art that would motivate one to combine the references as presented. "Before the PTO may combine the disclosures of two or more prior art references in order to

establish *prima facie* obviousness, there must be some **suggestion for doing so**....*In re Fine*, 837 F.2d 1071, 1074, 5 USPQ.2d 1596, 1598-99 (Fed. Cir. 1988)." [at 1943] (Emphasis added). "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification. *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127" [Fed. Cir. 1984] [at 1783].

Therefore, Applicants respectfully submit that the combination could only be justified by use of the benefit of impermissible hindsight vision afforded by the Applicants' claimed invention. The Federal Circuit has repeatedly cautioned against employing hindsight by using the applicant's disclosure as a blueprint to reconstruct the claimed invention out of isolated teaching of the prior art. *See, e.g., Grain Processing Corp. v. American-Maize Prods. Co.*, 5 U.S.P.Q.2d 1788, 1792 (Fed. Cir. 1988). That court has also cautioned against focusing on the obviousness of the differences between the claimed invention and the prior art rather than on the obviousness of the claimed invention as a whole as Section 103 requires. *See, e.g., Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 231 U.S.P.Q. 81, 93 (Fed. Cir. 1986), *cert. denied*, 480 U.S.P.Q. 947 (1987).

Regarding claims 37 through 39, the Examiner has stated that it is implied in the process of stereolithography that the stabilizers could assume several different heights or distances including a distance greater than or less than a minimum distance of at least one of said conductive structures. This, however, does not explain why one would be motivated to form stabilizers of the specific heights recited in claims 37 through 39, as Hull does not contemplate forming stabilizers, and Kuniaki uses support projections of the same form and size as the conductive structures.

Moreover, there is no teaching or suggestion in either Kuniaki or Hull of a method that includes forming a stabilizer to have a height less than a minimum distance a conductive structure protrudes from an active surface of a semiconductor die. Specifically, with respect to the teachings of Kuniaki, Kuniaki does not teach of suggest that a support projection 12 thereof may have a height less than a minimum distance a solder ball 11 protrudes from surface 4a.

Likewise, as both Kuniaki and Hull lack any teaching or suggestion of forming a stabilizer (*e.g.*, a support projection 12 of Kuniaki) to space an active surface (*e.g.*, surface 4a of Kuniaki) from a substrate a distance greater than a minimum distance a conductive structure (*e.g.*, a solder ball 11 of Kuniaki) protrudes from the active surface, it is respectfully submitted that Kuniaki and Hull do not render claim 38 obvious under 35 U.S.C. § 103(a).

Claim 39 is additionally allowable since neither Kuniaki nor Hull appears to teach or suggest employing a stabilizer structure to lengthen at least one conductive structure. In Kuniaki, the solder balls 11 and support projections 12 are both formed from solder. When the solder of the solder balls 11 is reflowed to establish electrical connections, the solder of the support projections would also likely be reflowed. It is, therefore, not understood how the support projections 12 of Kuniaki could cause solder balls 11 thereof to lengthen.

In view of the foregoing, Applicants respectfully submit the combination of Kuniaki and Hull fails to establish a *prima facie* case of obviousness, and under 35 U.S.C. § 103(a) claims 6, 7, 11, and 37 through 39 are allowable over the cited references.

Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki

Claims 9 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653). Applicants respectfully traverse this rejection, as hereinafter set forth.

For the reasons set forth above, Kuniaki fails to expressly or inherently describe the claim 1 limitation of "forming at least one stabilizer of a dielectric material securable to said active surface". Claims 9 and 12 depend from claim 1. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

Furthermore, claim 12 recites the limitation of "said forming said at least one stabilizer comprises applying a layer of photoresist material on said active surface and patterning said layer." The Examiner takes official notice that applying and patterning a photoresist layer is

conventionally practiced in the semiconductor industry, and would therefore be obvious. Applicants respectfully object to this finding, for while photoresist layers may be known in the industry, it is submitted that there is nothing in the references or the prior art that would render obvious the use of a photoresist layer *to form a stabilizer* on a flip-chip semiconductor die.

Applicants respectfully submit claims 9 and 12 are allowable over the present rejection under 35 U.S.C. § 103(a).

Obviousness Rejection Based on Japanese Patent No. 10189653 to Kuniaki in view of U.S. Patent No. 6,046,910 to Ghaem et al.

Claim 17 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuniaki (Japanese Patent No. 10189653) in view of Ghaem et al. (U.S. Patent No. 6,046,910). Applicants respectfully traverse this rejection, as hereinafter set forth.

Kuniaki fails to expressly or inherently describe the claim 1 limitation of "forming at least one stabilizer of a dielectric material securable to said active surface". Instead, Kuniaki has support projections 12 that are formed as conductive solder balls. The conductive pillars 44 of Ghaem et al. also fail to teach a stabilizer of a dielectric material (see col. 9, lines 1-13). The combination fails to teach or suggest all the claim limitations, and under 35 U.S.C. § 103(a) claim 17 is allowable as depending from claim 1.

Obviousness Rejection Based on U.S. Patent No. 6,046,910 to Ghaem et al. in view of U.S. Patent No. 4,575,330 to Hull

Claims 18, 19, and 41 through 49 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem et al. (U.S. Patent No. 6,046,910) in view of Hull (U.S. Patent No. 4,575,330). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 18 and 19 are both allowable, among other reasons, as depending from claim 1, which is allowable.

Claims 41 through 49 are each allowable, among other reasons, as depending from claim 36, which is allowable.

It is respectfully submitted that there are additional reasons that claims 18, 19 and 41 through 49 are allowable over the combination of Ghaem et al. and Hull.

Ghaem et al. describes an integrated circuit component 20 having bond pads 26 and conductive members 32, 44 in slidable communication with terminals 48 on a substrate 46 (see Figs. 1 and 7 and col. 5, lines 6-11). Integrated circuit component 20 is attached to substrate 46 via polymeric bodies 50, which hold conductive members 32, 44 in compressive communication with terminals 48 (see col. 6, lines 36-65 and col. 7, lines 1-18). In some embodiments, polymeric preforms 40 are formed on substrate 46 or integrated circuit component 20 to restrict the flow of a polymeric precursor of bodies 50 into the area between substrate 46 and integrated circuit component 20 (see col. 5, line 66 - col. 6, line 13). Polymeric preforms 40 are preferably formed of compressible material which does not significantly interfere with the shrinkage of polymeric bodies 50 (see col. 6, lines 14-17). Hull teaches an apparatus for production of three dimensional objects by stereolithography. There is no suggestion or motivation in the cited references or from the knowledge generally available in the prior art which would lead one of ordinary skill in the art to modify Ghaem et al. with the teachings of Hull, as has been presented.

The Examiner indicates one would be motivated to form the polymeric preforms 40 of Ghaem et al. with stereolithography as taught by Hull in order to precisely form insulative stabilizers. As discussed above, Applicants can find no evidence in Hull describing forming parts for microelectronic devices or any description of forming parts which are secured or attached to other items not formed by stereolithography, such as would be the case with the instant combination. Regarding Ghaem et al., polymeric preforms 40 are not for the purpose of stabilizing, but act as flow restrictors that prevent under-fill by polymeric bodies 50. This is born out by the fact that polymeric preforms 40 are not even necessary if polymeric bodies 50 are viscous and will not substantially flow during application (see col. 8, lines 39-43) Even if polymeric preforms 40 could be characterized as stabilizers, stereolithographically formed

stabilizers would not reduce any risk of short circuiting in Ghaem et al. Conductive members 32, 44 are uniquely formed to be in slidable communication with terminals 48 and are not attached to the substrate in such a way as to cause shorting problems. Accordingly, Applicants respectfully submit there would be no motivation for the present combination of Ghaem et al. and Hull.

Ghaem et al also teaches away from the asserted combination. Polymeric preforms 40 are formed of compressible material so that polymeric bodies 50 can shrink and urge conductive members 32, 44 into contact with terminals 48 (see col. 7, lines 15-19). This allows the conductive members 32, 44 to be slidable while maintaining good electrical contact. A rigid stereolithographically formed preform 40 would interfere with this type of electrical contact, and goes directly against the whole purpose of the Ghaem et al. invention.

In view of the foregoing, Applicants respectfully submit the cited references fail to establish a *prima facie* case of obviousness, and under 35 U.S.C. § 103(a) claims 18, 19, and 41 through 49 are allowable over Ghaem et al. and Hull.

Obviousness Rejection Based on U.S. Patent No. 6,046,910 to Ghaem et al. in view of U.S. Patent No. 4,575,330 to Hull and further in view of U.S. Patent No. 5,870,220 to Migdal et al.

Claims 20 through 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ghaem et al. (U.S. Patent No. 6,046,910) in view of Hull (U.S. Patent No. 4,575,330) and further in view of Migdal et al. (U.S. Patent No. 5,870,220). Applicants respectfully traverse this rejection, as hereinafter set forth.

Claims 20 through 30 are each allowable, among other reasons, as depending from claim 19.

In addition, Applicants respectfully submit the 35 U.S.C. § 103(a) obviousness rejections of claims 20 through 23 are improper because they fail to establish a prima facie case of obviousness.

Migdal relates generally to three-dimensional (3D) scanning and measuring systems, and relates particularly to a portable 3D scanning system and method which facilitate acquisition and

storage of data relating to 3D profiles of objects for subsequent computer-aided data processing and reproduction of the 3D profiles of the objects by shape digitizing and adaptive mesh generation (see col. 1, lines 6-12). It should be noted, contrary to the characterization found in the Office Action (page 7), Migdal does not disclose a stereolithography system. Reference to stereolithography was only made once in the entire patent to illustrate an application of the scanning system taught and disclosed (see col. 4, line 15). Moreover, Migdal includes no description of the use of a machine vision system to recognize the location on a substrate at which at least one stabilizer or, for that matter, any other structure is to be formed.

Accordingly, Applicants respectfully submit there would be no motivation for the suggested combination of Migdal et al. with Ghaem et al. and Hull et al., and that the cited references, alone or in combination, fail to teach or suggest all of the claim limitations. Under 35 U.S.C. § 103(a), claims 20 through 23 are therefore allowable.

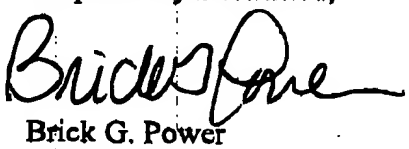
ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 18, 19 and 36 through 41 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1 through 23 and 36 through 49 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,



Brick G. Power
Registration Number 28,265
Attorney for Applicants
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

Date: May 7, 2002

BGP/hlg:djp
Enclosure: Version With Markings to Show Changes Made

N:\2269\3936\Amendment Final.wpd

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Three times amended) A method of forming a flip-chip semiconductor die, comprising:

providing at least one flip-chip semiconductor die having an active surface; and

forming at least one stabilizer comprising a dielectric material and securing said at least one stabilizer [securable] to said active surface so as to protrude from said active surface, said at least one stabilizer being [an unitary structure of any desired shape and] configured to at least partially stabilize an orientation of said at least one flip-chip semiconductor die when disposed face down over a higher level substrate.

18. (Three times amended) A method of fabricating a semiconductor device component, comprising:

providing at least one semiconductor substrate with contact pads on an active surface thereof; and

sequentially forming on said active surface at least one stabilizer [of any desired shape] having a plurality of superimposed, contiguous, mutually adhered layers of photopolymer, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device component upon being disposed face down over a higher level substrate.

19. (Three times amended) A method of fabricating a semiconductor device component, comprising:

placing at least one semiconductor substrate having an active surface with contact pads exposed thereon in a horizontal plane;

recognizing a location and orientation of said at least one substrate;

stereolithographically forming on said active surface, between one of said contact pads and a peripheral edge of said at least one substrate, at least one stabilizer [of any desired shape] comprising at least one layer of an electrically nonconductive semisolid material.

36. (Three times amended) A method for electrically bonding a flip-chip semiconductor device component having a surface and conductive structures protruding from said surface to a substrate having contacts positioned correspondingly to said conductive structures, said method comprising:

forming at least one [unitary] stabilizer structure [of any desired shape] comprising a dielectric material configured to be disposed between said surface and said substrate;

inverting and positioning said semiconductor device component on said substrate to contact said conductive structures to corresponding contacts; and

bonding said conductive structures to the corresponding contacts.

37. (Three times amended) The method of claim 36, wherein said forming at least one [unitary] stabilizer structure comprises forming said at least one [unitary] stabilizer structure to have a height less than a minimum distance said conductive structures protrude from said surface.

38. (Three times amended) The method of claim 36, wherein said forming at least one [unitary] stabilizer structure comprises forming said at least one [unitary] stabilizer structure to space said surface from said substrate a distance greater than a minimum distance at least one of said conductive structures protrudes from said surface.

39. (Three times amended) The method of claim 38, wherein said bonding comprises employing said at least one [unitary] stabilizer structure to lengthen at least one of said conductive structures.

40. (Three times amended) The method of claim 36, wherein said forming at least one [unitary] stabilizer structure comprises configuring said at least one [unitary] stabilizer structure to be positioned between a periphery of said surface of said semiconductor device component and said conductive structures.

41. (Amended) A method of forming a flip-chip semiconductor die, comprising:

providing at least one flip-chip semiconductor die having an active surface with contact pads exposed thereon;

applying a layer of a partially uncured photopolymer to said flip-chip semiconductor; and

stereolithographically forming on said flip-chip semiconductor, between one of said contact pads and a peripheral edge of said flip-chip semiconductor, at least one stabilizer securable to said active surface so as to protrude from said active surface, said at least one stabilizer being [an unitary] a structure [of any desired shape and] configured to at least partially stabilize an orientation of said at least one flip-chip semiconductor die when disposed face down over a higher level substrate.